61

## REMARKS

Claim 5 is being amended in order to place the case in condition for appeal. This amendment is made to correct a typographical error appearing in the text of the amended claim.

Respectfully submitted,

William O. Geny

Applicant:

**Brian DONOVAN** 

Serial Nº:

09/410,202

Filed:

September 30, 1999

Title:

ZERO OVERHEAD COMPUTER INTERRUPTS WITH

TASK SWITCHING

Group Art Unit: 2783
Examiner: D. Eng

Deletions are bracketed; additions are underlined.

The following material shows the manner of amendment of the specification.

5. The interrupt and task change processing circuit of claim 4 wherein said task priority selection circuit includes a variable rate task priority incrementing circuit for varying an assigned priority of a task such that said priority increases with time, whereby its execution is caused [by] to occur within a predetermined period of time.

RECEIVED

OCT 1 6 2002

Technology Center 2100